C1 Cmd

openings because the ions approaching the wafer at the angles near 90° are less likely to create overhangs near the top of the openings.

C2

[0032] Dielectric 534 (Figs. 7A, 7B) on the sidewalls of stacks 532 insulates the control and floating gates from polysilicon wordlines 536. In some embodiments, dielectric 534 includes silicon dioxide (not separately shown) formed on the sidewalls of polysilicon 524, 528, and also includes an outer layer consisting of silicon nitride spacers which overlie the silicon dioxide. A thin silicon dioxide layer 535 (Fig. 7A) is formed on the substrate under the dielectric 534.

[0035] A thin silicon dioxide layer 550 is shown to overlie the bitline regions 542. This layer is removed during the formation of the contact openings for contacts 548.

C3

Enclosed as Appendix A is a copy of specification paragraphs 8, 32, and 35 annotated to indicate the changes to these paragraphs. In the annotated specification paragraphs, added material is in bold, and deleted material is in brackets.

IN THE CLAIMS

Amend Claims 17, 20, 21, and 23 to read:

C4

--17. (Amended) The method of Claim 8 wherein:

the body comprises (a) a region consisting largely of silicon and (b) a silicon oxide layer situated along the silicon region; and

the reacting act includes causing oxygen in the silicon oxide layer to be dissolved by titanium of the titanium layer.

C5

20. (Amended) The method of Claim 18 wherein:

the first region comprises (a) a substrate region consisting largely of silicon and (b) a silicon oxide layer extending along the silicon substrate region at least at the bottom of the opening; and

the reacting act includes causing oxygen of the silicon oxide layer at the bottom of the opening to be dissolved by titanium of the titanium layer.

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